UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/570,665	03/06/2006	Akihiko Endo	P29120	1241

7055 7590 04/08/2008

GREENBLUM & BERNSTEIN, P.L.C.
1950 ROLAND CLARKE PLACE
RESTON, VA 20191

EXAMINER	
HUNG, MING HUNG	
ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
04/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com
pto@gbpatent.com

Office Action Summary	Application No.	Applicant(s)	
	10/570,665	ENDO ET AL.	
	Examiner	Art Unit	
	MING HUNG HUNG	4158	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Preliminary amendment received on 03/06/06 has been entered into record. Claims 1-13 are pending.

Priority

2. Examiner acknowledged that this application 10/570,665 files on 03/06/06 claims the benefit to the foreign application 2003-315986 files on 09/08/03. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file

Specification

3. The specification is objected to because of the following informalities:

a. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

b. Page 4, lines 28-30, "either one of the fitting surface of the active layer wafer and the fitting surface of the supporting wafer" should read "either one of the fitting surface of the active layer wafer or the fitting surface of the supporting wafer". Similar errors have been found in the rest of the specification.

Appropriate action is required.

Claim Objections

4. Claims 2-4 are objected to because of the following informalities:

a. As to claims 2 and 4, lines 2-3, "either one of said fitting surface of said active layer wafer and said fitting surface of said supporting wafer" should read "either one of

said fitting surface of said active layer wafer or said fitting surface of said supporting wafer".

b. As to claim 3, line 3, "the epitaxial growth method" lacks antecedent basis.

Appropriate action is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriceau et al. (6,756,285 B1 and Moriceau hereinafter).

7. As to claim 1, Moriceau discloses a multilayer structure with controlled internal stresses and making same comprising:

a manufacturing method of a bonded wafer (col. 1, lines 6-22), **in which the bonded wafer is manufactured by bonding a wafer for active layer wafer** (the first main layer 110a, Fig. 7) **with a supporting wafer** (the second main layer 110b, Fig 7)**, where the active layer wafer and the supporting wafer, which are to be bonded together** (col. 10, lines 16-19)**, have fitting surfaces, respectively, for fitting to each other** (silicon nitride film 130 and silicon

oxide film 120 as shown in Fig. 7)**, each of the fitting surfaces comprising a part of a spherical surface having the same curvature** (Fig. 7; when the first main layer 110a and the second main layer 110b, each having the same curvature, are bonded together, the interface between the silicon oxide film 120 and the silicon nitride film 130 is a spherical surface and each the first main layer 110a and the second main layer 110b is a part of the spherical surface)**.**

8. As to claim 6**,** Moriceau discloses a multilayer structure with controlled internal stresses and making same comprising:

ion-implanting of hydrogen gas or noble gas into the active layer wafer to form an ion-implanted layer in the active layer wafer (112, Fig. 7; col. 9, lines 42-49)**; subsequently bonding the active layer wafer with the supporting wafer to form the bonded wafer** (col. 10, lines 16-19)**; and then heat treating the bonded wafer by holding it at a predetermined temperature so as to induce a cleavage and separation at the site of ion-implanted layer as an interface** (col. 10, lines 23-34)**.**

9. As to claim 7, Moriceau discloses a multilayer structure with controlled internal stresses and making same comprising:

a bonded wafer manufactured by bonding an active layer wafer (first main layer 110a, Fig. 7) **with a supporting wafer** (second main layer 110b, Fig. 7)**, in which the active layer wafer and the supporting wafer, which are to be bonded together** (col. 10, lines 16-19)**, have fitting surfaces, respectively, for fitting to each other** (silicon nitride film 130 and silicon oxide film 120 as shown in Fig. 7)**, each of the fitting surfaces comprising a part of a**

spherical surface having the same curvature (Fig. 7; when the first main layer 110a and the second main layer 110b, each having the same curvature, are bonded together, the interface between the silicon oxide film 120 and the silicon nitride film 130 is a spherical surface and each the first main layer 110a and the second main layer 110b is a part of the spherical surface)**.**

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 2-5 and 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriceau in view of Kuwahara et al. (2001/0029072 A1) and Nakazato et al. (US Patent No. 5,071,785 and Nakazato hereinafter).

12. As to claims 2, 3, 5 and 8, although Moriceau discloses substantial features of the claimed invention (see paragraphs above), it fails to disclose:

in which at least either one of the fitting surface of the active layer wafer and the fitting surface of the supporting wafer includes a hetero structure along a thickness-wise direction [claim 2];

in which said hetero structure is provided along the thickness-wise direction in the epitaxial growth method [claim 3];

in which the hetero structure is disposed in a top and a back surfaces, respectively, of the active layer wafer or the supporting wafer, and the hetero structure in the top and the back surfaces are different in thickness from each other [claims 5 and 8].

Nonetheless, these features are well known in the art and would have been an obvious modification of the method disclosed by Moriceau, as evidenced by Kuwahara.

Kuwahara discloses a method of recycling a delaminated wafer and silicon wafer used for the recycling comprising:

in which at least either one of the fitting surface of the active layer wafer and the fitting surface of the supporting wafer includes a hetero structure along a thickness-wise direction (oxide layer 3 and epitaxial layer 13 together form the hetero structure as shown in Fig. 1b) **[claim 2]** to form an SOI layer after bonding separation**;**

in which the hetero structure is provided along the thickness-wise direction in the epitaxial growth method ([0054], lines 5-7, the epitaxial layer 13 in the hetero structure was

formed in a epitaxial growth method) **[claim 3]** to reprocessing the epitaxial wafer many times for reuse;

in which the hetero structure is disposed in a top and a back surfaces, respectively, of the active layer wafer or the supporting wafer, (the hetero structured formed by oxide layer 3 and epitaxial layer 13 is disposed on the active layer wafer represented by bond wafer 2 as shown in Figs. 1a-1c) **and the hetero structure in the top and the back surfaces are different in thickness from each other** (top surface of bond wafer 2 containing oxide layer 3 and epitaxial layer 13 is thicker than the back surface of bond wafer 2 containing oxide layer 3) **[claims 5 and 8]** to form an SOI layer with high crystal quality and high thickness uniformity.

Given the teaching of Kuwahara, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying the method disclosed in Moriceau by employing the well known and conventional features of a hetero structure that is provided in a epitaxial method, such as disclosed by Kuwahara, in order to improve the productivity of the SOI wafer having high quality SOI layer and cost reduction can be achieved.

However, the Examiner notices that the structure in Fig. 1 of Kuwahara does not have a spherical surface and the oxide layer 3 might prevent the bond wafer from warping before bonding as required by claim 1, therefore, not combinable with Moriceau or destroys Moriceau. Nonetheless, Nakazato discloses a method for preparing a substrate for forming semiconductor devices by bonding warped wafers comprising:

pre-warping a similar structure as the structure in Fig. 1 of Kuwahara before bonding (Fig. 1A, col. 4, lines 12-23).

Given the teaching of Nakazato, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying the method disclosed by Moriceau in view Kuwahara by employing the well known and conventional features of pre-warping, such as disclosed by Nakazato, in order to form a semiconductor device with an SOI structure which is free from warp and exhibits high precision in flatness.

Accordingly, it would have been obvious to a person having ordinary skills in the art at the time of the invention to modify the method disclosed in Moriceau by employing the techniques disclosed in Kuwahara and Nakazato in order to obtain the advantages found in both techniques (high quality SOI layer, cost reduction, and an SOI layer that is free from warp).

13. As to claims 10, 11 and 13, Moriceau discloses a multilayer structure with controlled internal stresses and making same comprising:

ion-implanting of hydrogen gas or noble gas into the active layer wafer to form an ion-implanted layer in the active layer wafer (112, Fig. 7; col. 9, lines 42-49)**; subsequently bonding the active layer wafer with the supporting wafer to form the bonded wafer** (col. 10, lines 16-19)**; and then heat treating the bonded wafer by holding it at a predetermined temperature so as to induce a cleavage and separation at the site of ion-implanted layer as an interface** (col. 10, lines 23-34).

14. Claims 4, 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriceau in view of Linn et al. (5,362,667 and Linn hereinafter) and Nakazato.

15. As to claims 4 and 9, although Moriceau discloses substantial features of the claimed invention (see paragraphs above), it fails to disclose:

in which at least either one of the fitting surface of the active layer wafer and the fitting surface of the supporting wafer includes an insulating film along a thickness-wise direction [claim 4];

in which the insulating film is disposed in a top surface and a back surface, respectively, of the active layer wafer or the supporting wafer, and the insulating film in the top and the back surfaces are different in thickness from each other [claim 9].

Nonetheless, these features are well known in the art and would have been an obvious modification of the method disclosed by Moriceau, as evidenced by Linn.

Linn discloses a bonded wafer processing comprising:

in which at least either one of the fitting surface of the active layer wafer and the fitting surface of the supporting wafer includes an insulating film along a thickness-wise direction (oxide 706 and nitrox 707, or oxide 716 and nitrox 717, together form the insulating film on the wafer 702, or 712, as shown in Fig. 7a) **[claim 4]** to form an SOI structure after bonding separation**;**

in which the insulating film is disposed in a top surface (oxide 706 and nitrox 707 or oxide 716 and nitrox 717 as shown in Fig. 7a) **and a back surface** (oxide 704 or 714 as shown in Fig. 7a)**, respectively, of the active layer wafer** (device wafer 702, Fig. 7a) **or the supporting wafer** (handle wafer 712, Fig. 7a)**, and the insulating film in the top and the back surfaces are different in thickness from each other** (the thickness of oxide 706 and nitrox 707,

or oxide 716 and nitrox 717, is thicker than the oxide 704, or 714, as shown in Fig. 7a) **[claim 9]** to neutralize the positive charges at the interface generated by radiation**.**

Given the teaching of Linn, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying the method disclosed in Moriceau by employing the well known or conventional features of using different thickness insulating films, such as disclosed by Linn, in order to improve the SOI structure's radiation hardness.

Examiner notices that the structure in Fig. 7a of Linn does not have a spherical surface and the structure in Fig. 7a of Linn might prevent the wafers from warping before bonding as required by claim 1, therefore, not combinable with Moriceau or destroys Moriceau. Nonetheless, Nakazato discloses a method for preparing a substrate for forming semiconductor devices by bonding warped wafers comprising:

pre-warping a similar structure as the structure in Fig. 7a of Linn before bonding (Fig. 1A, col. 4, lines 12-23).

Given the teaching of Nakazato, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying the method disclosed by Moriceau in view of Linn by employing the well known and conventional features of pre-warping, such as disclosed by Nakazato, in order to form a semiconductor device with an SOI structure which is free from warp and exhibits high precision in flatness.

Accordingly, it would have been obvious to a person having ordinary skills in the art at the time of the invention to modify the method disclosed in Moriceau by employing the techniques disclosed in Linn and Nakazato in order to obtain the advantages found in both

techniques (improving the SOI structure's radiation hardness and an SOI structure that is free from warp).

16. As to claim 12, Moriceau discloses a multilayer structure with controlled internal stresses and making same comprising:

ion-implanting of hydrogen gas or noble gas into the active layer wafer to form an ion-implanted layer in the active layer wafer (112, Fig. 7; col. 9, lines 42-49)**; subsequently bonding the active layer wafer with the supporting wafer to form the bonded wafer** (col. 10, lines 16-19)**; and then heat treating the bonded wafer by holding it at a predetermined temperature so as to induce a cleavage and separation at the site of ion-implanted layer as an interface** (col. 10, lines 23-34).

Contact Information

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ming Hung Hung whose telephone number is (571)270-3832. The examiner can normally be reached on Monday through Friday 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Walter Benson can be reached on (571)272-2227. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ming Hung Hung/
Examiner, Art Unit 4158

/Uyen-Chau N. Le/
Primary Examiner, Art Unit 4158